

DERWENT-ACC-NO: 2002-255858

DERWENT-WEEK: 200258

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TITLE: Lead frame for semiconductor package, has die pad  
on which  
semiconductor chip having power electrode pads are  
electrically interconnected  
to side ring pads by power bonding wires

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PATENT-FAMILY:

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PAGES	MAIN-IPC	
KR 2002016241	March 4, 2002	N/A
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APPLICATION-DATA:

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APPL-DATE		
KR2002016241A	N/A	2000KR-0049460
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US20020024122A	N/A	2001US-0909736
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INT-CL (IPC): H01L023/495

ABSTRACTED-PUB-NO: US20020024122A

BASIC-ABSTRACT: NOVELTY - A lead frame comprises a die pad (12) on which semiconductor chip (20) having multiple electrode pads (22), is mounted. A tie bar connects the die pad and a side ring pad (18) arranged in between die pad (14). The power electrode pads (22a) and the inner leads (14).

are electrically connected to side ring pads by power bonding wires (30).

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor package.

USE - Lead frame for semiconductor package (claimed) e.g. chip size package (CSP).

ADVANTAGE - Improves high frequency characteristics and grounding capacity using lead frame. Reduces noises and enhances flexibility of bonding wires. Provides fine lead and high pin-count requirements at lower cost.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor package.

Die pad 12

Inner lead 14

Side ring pad 18

Semiconductor chip 20

Electrode pad 22

Power electrode pad 22a

Power bonding wire 30

CHOSEN-DRAWING: Dwg.2/7

TITLE-TERMS:  
LEAD FRAME SEMICONDUCTOR PACKAGE DIE PAD SEMICONDUCTOR CHIP  
POWER ELECTRODE PAD  
ELECTRIC INTERCONNECT SIDE RING PAD POWER BOND WIRE

DERWENT-CLASS: U11

EPI-CODES: U11-D01; U11-D03A1A;

SECONDARY-ACC-NO:

Non-CPI Secondary Accession Numbers: N2002-197881